Abstract

An improved cascaded biquad infinite impulse response (IIR) filter structure is provided. The IIR filter of the invention may be implemented in a digital signal processor (DSP) such as a very long instruction word (VLIW) type DSP, as well as other processing circuitry, e.g., an integrated circuit. The new filter structure, among other advantages, overcomes the bottleneck condition known to occur in the updating operation of the $w_2(n-1)$ state of a conventional cascaded biquad IIR filter. In one illustrative implementation of the invention, this is accomplished by adding a single 32-bit intermediate state thus providing a cascaded biquad IIR filter structure such that the $w_2(n-1)$ state may be updated one clock cycle earlier. Thus, in a StarCore SC140 DSP example where a corresponding conventional cascaded biquad IIR filter structure executes at seven cycles per input sample, the improved cascaded biquad IIR filter structure of the present invention executes at six cycles per input sample. Therefore, without losing any precision, the kernel cycle count associated with the improved cascaded biquad IIR filter structure is advantageously reduced by 14 percent. Such a reduction in kernel count translates to a proportional increase in the processing speed of the DSP or other processing circuitry with which it is implemented.